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EdkDSP reprogrammable floating point accelerators on Kintex FPGA with HDMI

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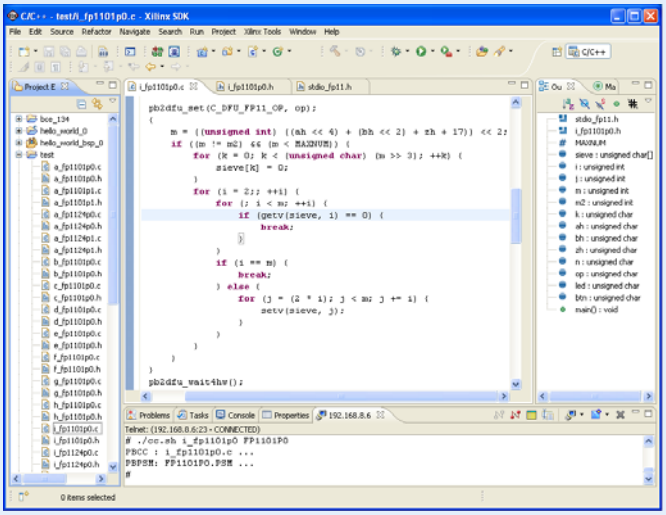
- We present the EdkDSP reprogrammable floating point accelerators on the 45nm Xilinx Spartan 6 FPGA (SP605, PLB bus) and the 28nm Xilinx Kintex FPGA (KC705, AXI-4 bus). The Kintex SoC supports the HDMI 1080p60 video I/O based on the HDMI ON Semicond. image sensor.
- The Spartan SoC design is based on MicroBlaze and the Non-MMU PetaLinux. The finite state machines (FSMs) for the EdkDSP accelerators are compiled on the SP605 board in run-time. The SP605 design combines a 600 MFLOPs EdkDSP accelerator and 1080i60 DVI output.
- The EdkDSP floating point accelerators use reprogrammable FSMs. The FSMs are implemented as on-fly reconfigurable 8-bit soft processors (Xilinx PicoBlaze KCPSM3). Processors are reprogrammable by change of the firmware. The MicroBlaze on the SP605 compiles this firmware by background execution of UTIA EdkDSP C compiler in the real-time.
- The Kintex SoC is controlled by the 32bit MicroBlaze soft-core supporting the LwIP TCP-IP file transfer, WWW server and local file system on top of the Xilkernel OS. The design is using the 512 bit wide AXI-4 buses and several independent VDMA controllers. This enables system clock 150 MHz with one HDMI 1920x1080p60 display controller and in parallel supports 4 HDMI 1920x1080p60 video streams.
- The corresponding 4 independent video frame buffers support sustained 24 Gbit/s RD and parallel 24 Gbit/s WR from/to the 800 MHz MICRON DDR3. The video chain is combined with four on-fly firmware reprogrammable single-precision 8xSIMD accelerators at 150 MHz delivering sustained 4 GFLOPs DSP performance. We use the Xilinx ISE 14.4 tools.
- The Kintex system is being developed for the e-car safety-electronic in the project IDEAS. We acknowledge support by ENIAC and MEYS CZ.

EdkDSP firmware can be compiled directly on the SP605 kit from C.



EdkDSP with DVI 1080i60 video output on the Xilinx SP605 kit

EdkDSP with the HDMI 1080p60 video chain on the Xilinx KC705 kit

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